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09/599,938	06/23/2000	Joseph Herbst	108339-09032	9234
32294	7590	03/03/2006		EXAMINER
SQUIRE, SANDERS & DEMPSEY L.L.P. 14TH FLOOR 8000 TOWERS CRESCENT TYSONS CORNER, VA 22182			MEW, KEVIN D	
			ART UNIT	PAPER NUMBER
			2664	

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Please find below and/or attached an Office communication concerning this application or proceeding.

SF

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/599,938	HERBST, JOSEPH
	<b>Examiner</b>	<b>Art Unit</b>
	Kevin Mew	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 24 January 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-26 and 28-33 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 12-16, 18-26, 28, 31-33 is/are allowed.  
 6) Claim(s) 1-11 and 29 is/are rejected.  
 7) Claim(s) 17 and 30 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 6/23/2000 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

***Detailed Action***

***Response to Amendment***

1. Applicant's Remarks/Arguments filed on 1/24/2006 regarding claims 1-10 have been fully considered and claims 1-26, 28-33 are currently pending. Claim 27 has been canceled by applicant.
  
2. Acknowledgement is made of the amended claims 1, 6 and 7.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 29 recites the limitation "storing a first cell in the local memory" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim because it is unclear as to whether what the local memory refers to in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Headrick et al. (USP 5,724,358).

Regarding claim 1, Headrick discloses a network switch to perform a method for storing data (**ATM switch**, see col. 3, lines 6-7 and element 82, Fig. 5) comprising:

at least one port data port interface (**Buffering and Routing unit**, see element 124, Fig. 5);

a first memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10);

a second memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10); and

a memory management unit (**Buffer Manager unit and Routing and Buffering unit**, see elements 128, 126, Figs. 5 and 7; note that the combination of Buffer Manager unit and Routing and Buffering unit is interpreted as a memory management unit) in connection-with said at least one data port interface (**Buffer Manager in connection with Routing and Buffering unit**, see element 126, Fig. 5), said first memory (**the portion of the Cell Buffer Memory**

**pointed to by the Pointer Memory 178, see Fig. 7), and said second memory (the portion of the Cell Buffer Memory pointed to by the Pointer Memory 180, see Fig. 7),**

**wherein the memory management unit (Buffering and Routing unit of the memory management unit, see element 126, Fig. 7) receives data from the at least one data port interface (Buffering and Routing receives data from the Input Translation, see Figs. 5 and 7), determines if the data is to be stored in one of the first memory or the second memory (a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7), stores the data in one of the first memory or the second memory as a linked list (pointer memories 178, 180, pointing to the Cell Buffer Memory, contain a plurality of linked list type data structures that are output queues for the plurality of output ports, see col. 8, lines 61-67), retrieves the data from one of the first memory or the second memory (data are retrieved from the corresponding cell buffers of the Cell Buffer Memory pointed to by pointer memories 178, 180 as output queues, see col. 8, lines 61-63), and forwards the data for egress (the Buffering and Routing unit 126 is forwarding the data for output to the Output Translation, see Fig. 5 and 7),**

**wherein the memory management unit (the combined system of Buffer Manager 128 and Routing and Buffering Unit 126, Figs. 5 and 7) further comprises a communication channel (data line for communicating data from Buffer Manager 128 to Routing and**

**Buffering Unit 126**, Fig. 7) and a data input section in connection with the communication channel (**the data input section that comprises data paths #1, #2, #3, #4**, Fig. 7), and wherein the data input section (**the data input section that comprises data paths #1, #2, #3, #4**, Fig. 7) further comprises at least one cell accumulation buffer (**data paths #1, #2, #3, #4**, Fig. 7) and a slot assembly unit (**Cell Buffer Memory 174**, Fig. 7) being configured to receive cells (**receives ATM cells**, col. 7, lines 49-67, col. 8, lines 1-10 and Fig. 7) from the at least one cell accumulation buffer (**from data paths**, col. 7, lines 38-48) and package the received cells into cell slots (**the cells received are stored in cell slots**, Fig. 10) to be stored in the second memory (**ATM cells for ports 7-15 are stored in the respective memory buffers located in the Cell Buffer Memory 126 pointed to by Pointer Memory 180**, see col. 7, lines 25-37 and Figs. 7 and 10).

Regarding claim 2, Headrick discloses a network switch as recited in claim 1, said network switch further comprising

a status location budget manager (**Buffer Manager unit**, see element 128, Figs. 7) in connection with the at least one data port interface (Buffering and Routing unit, see element 126, Fig. 7), the first memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10) and the second memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10), for determining if the data is to be stored in the first memory or the second memory (**a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to**

**store data cells for ports 0-7, and a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7).**

Regarding claim 3, Headrick discloses a network switch as recited in claim 1, said network switch further comprising

a first memory controller (**Memory Manager 1**, see element 170, Fig. 7) for storing data within said first memory (**storing data in the cell buffer memory pointed to by the Pointer Memory 178**, see Fig. 7) and a second memory controller (**Memory Manager 2**, see element 172, Fig. 7) for storing data within said second memory (**storing data in the cell buffer memory pointed to by the Pointer Memory 180**, see element 180, Fig. 7).

Regarding claim 4, Headrick discloses a network switch as recited in claim 1, wherein said first memory further comprises on-chip memory (**a memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 178 is an on-chip memory with respect to the Cell Buffer Memory**, see Fig. 7).

Regarding claim 5, Headrick discloses a network switch as recited in claim 1, wherein said second memory further comprises off-chip memory (**a memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 180 is off-chip memory with respect to the Buffer Manager 128**, see Fig. 5).

Regarding claim 6, Headrick discloses a network switch as recited in claim 1, wherein the memory management unit (**Buffer Manager unit and Routing and Buffering unit**, see elements 128, 126, Figs. 5 and 7; note that the combination of Buffer Manager unit and Routing and Buffering unit is interpreted as a memory management unit) further comprises:

a data output section (**data path units of the Routing and Buffering unit outputs data**, see elements 182, 184, 186, 188, Fig. 7; note that data output section is interpreted to comprise Output Layer, Output Translation, Routing and Buffering, see Fig. 5) in connection with the communication channel (**data paths in connection with the data arrow coming into element 126, Fig. 7**);

a first memory controller (**Memory Manager 1**, see element 170, Fig. 7) in connection with the first memory (**Memory Manager 1 in connection with a memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 178**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10, see Fig. 7), the data input section (**Memory Manager 1 in connection with data paths receiving data via the Cell Buffer Memory 126**, see elements 170, 182, 184, 186, 188, Fig. 7), and the data output section (**Memory Manager 1 in connection with data paths outputting data via the Cell Buffer Memory 126**, see elements 170, 182, 184, 186, 188, Fig. 7);

a second memory controller (**Memory Manager 2**, see element 172, Fig. 7) in connection with the second memory (**Memory Manager 2 in connection with a memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 178**, see col. 7, lines 25-37 and Fig. 7 and Fig. 10), the data input section (**Memory Manager 2 in connection with data paths receiving data via the Cell Buffer Memory**, see elements 172, 182, 184, 186, 188,

Fig. 7), and the data output section (**Memory Manager 2 in connection with data paths outputting data via the Cell Buffer Memory**, see elements 172, 182, 184, 186, 188, Fig. 7); at least one address pool (**Free List Memory**, see col. 7, lines 14-17 and element 176, Fig. 7; Free List Memory stores a plurality of pointers linking all free locations in cell buffer memory together so that a list of every free memory location is available) in connection with the first memory controller (**Memory Manager 1**, Fig. 7) and the second memory controller (**Memory Manager 2**, see Fig. 7); and a scheduler (**Memory Manager 1 schedules output queues for ports 0 through 7 to be stored in pointer memory 178**, see col. 7, lines 1-3 and col. 8, lines 66-67) in connection with the data input section (**data path units receiving data**, see elements 182, 184, 186, 188, Fig. 7) and the data output section (**data path units outputting data**, see elements 182, 184, 186, 188, Fig. 7).

Regarding claim 7, Headrick discloses a network switch as recited in claim 6, wherein the data input section further comprises:

a cell assembly unit (**Output Translation System for assembling ATM cells**, see col. 6, lines 9-27 and element 130, Fig. 5) in connection with the communication channel (**communication channel for data coming into data paths of the Buffering and Routing unit 126**, see data arrow coming into element 126, Fig. 7); a status location budget manager (Buffer Manager, see element 128, Fig. 7) in connection with the cell assembly unit (**Buffer Manager is in-connection with the Output Translation via the CPU**, see element 130, Fig. 5); and

at least one address pool (**Free List Memory**, see element 176, Fig. 7) in connection with the status location budget manager (**Buffer Manager**, see Fig. 7), the slot assembly unit (**Free List Memory in connection with Output Layer 132 via the Routing and Buffering unit**, see Figs. 5 and 7) and the data output section (**Free List Memory in connection with the data output section comprising Output Translation 130, Output Layer 132 via the Routing and Buffering unit**, see Figs. 5 and 7).

Regarding claim 8, Headrick discloses a network switch as recited in claim 7, wherein the cell assembly unit converts data received from the communication channel into a cell header format (**ATM cell has header field HEC**, see col. 6, lines 15-17 and Fig. 4), a cell data format (**information field**, see Fig. 4), and a sideband information format (**PT field distinguishes between cells containing user data and network information**, see col. 5, lines 1-38 and Fig. 4).

Regarding claim 9, Headrick discloses a network switch as recited in claim 7, wherein the status location budget manager (**Buffer Manager**, see element 128, Fig. 7) determines whether data received by the cell accumulation buffer is to be stored in the first memory or the second memory (**a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15**, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7).

Regarding claim 10, Headrick discloses a network switch as recited in claim 7, wherein the at least one cell accumulation buffer collects data (**Routing and Buffering unit collects data, see Fig. 7**) to be stored in the second memory (**stores data in buffer pointed to by Pointer Memory 180 in the Cell Buffer Memory, see Fig. 7**) prior to sending the data to be stored in the second memory to the slot assembly unit (**data are stored in the portion of the Celk buffer Memory pointed to by Pointer Memory 180 prior to sending the data to the Output Layer 132, see Fig. 7**).

Regarding claim 11, Headrick discloses a network switch to perform a method for storing data (ATM switch, see col. 3, lines 6-7 and element 82, Fig. 5) comprising:

at least one port data port interface (**Buffering and Routing unit, see element 124, Fig. 5**);  
a first memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178, see col. 7, lines 25-37 and Fig. 7 and Fig. 10**);  
a second memory (**a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180, see col. 7, lines 25-37 and Fig. 7 and Fig. 10**); and  
a memory management unit (**Buffer Manager unit and Routing and Buffering unit, see elements 128, 126, Figs. 5 and 7; note that the combination of Buffer Manager unit and Routing and Buffering unit is interpreted as a memory management unit**) in connection-with said at least one data-port-interface (**Buffer Manager in connection with Routing and Buffering unit, see element 126, Fig. 5**), said first memory (**the portion of the Cell Buffer Memory**

**pointed to by the Pointer Memory 178, see Fig. 7), and said second memory (the portion of the Cell Buffer Memory pointed to by the Pointer Memory 180, see Fig. 7),**

**wherein the memory management unit (Buffering and Routing unit of the memory management unit, see element 126, Fig. 7) receives data from the at least one data port interface (Buffering and Routing receives data from the Input Translation, see Figs. 5 and 7), determines if the data is to be stored in one of the first memory or the second memory (a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7), stores the data in one of the first memory or the second memory as a linked list (pointer memories 178, 180, pointing to the Cell Buffer Memory, contain a plurality of linked list type data structures that are output queues for the plurality of output ports, see col. 8, lines 61-67), retrieves the data from one of the first memory or the second memory (data are retrieved from the corresponding cell buffers of the Cell Buffer Memory pointed to by pointer memories 178, 180 as output queues, see col. 8, lines 61-63), and forwards the data for egress (the Buffering and Routing unit 126 is forwarding the data for output to the Output Translation, see Fig. 5 and 7),**

**wherein the memory management unit (the combined system of Buffer Manager 128 and Routing and Buffering Unit 126, Figs. 5 and 7) further comprises a communication channel (data line for communicating data from Buffer Manager 128 to Routing and**

**Buffering Unit 126**, Fig. 7) and a data input section in connection with the communication channel (**the data input section that comprises data paths #1, #2, #3, #4**, Fig. 7), a data output section (**a data section that comprises data paths #1, #2, #3, #4**, Fig. 7) in connection with the communication channel (**a data line going out from data paths and labeled as Output**, Fig. 7); a first memory controller (**Memory Manager #1**, Fig. 7) in connection with the first memory (**in connection with a first memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 178**, see col. 7, lines 25-37 and Figs. 7 and 10), the data input section (**incoming data into data paths**, Fig. 7), and the data output section (**outgoing data from data paths**, Fig. 7); a second memory controller (**Memory Manager #2**, Fig. 7) in connection with the second memory (**in connection with a second memory buffer in the Cell Buffer Memory 126 pointed to by Pointer Memory 180**, see col. 7, lines 25-37 and Figs. 7 and 10), the data input section (**incoming data into data paths**, Fig. 7), and the data output section (**outgoing data from data paths**, Fig. 7); at least one address pool (**Free List Memory**, see col. 7, lines 14-17 and element 176, Fig. 7; Free List Memory stores a plurality of pointers linking all free locations in cell buffer memory together so that a list of every free memory location is available) in connection with the first memory controller (**Memory Manager #1**, Fig. 7) and the second memory controller (**Memory Manager #2**, see Fig. 7); and a scheduler (**Memory Manager #1 schedules output queues for ports 0 through 7 to be stored in pointer memory 178**, see col. 7, lines 1-3 and col. 8, lines 66-67) in connection

with the data input section (**data path units receiving data**, see elements 182, 184, 186, 188, Fig. 7) and the data output section (**data path units outputting data**, see elements 182, 184, 186, 188, Fig. 7); and

wherein the data input section (**data path units receiving data**, see elements 182, 184, 186, 188, Fig. 7) further comprises:

a cell assembly unit (**Output Translation for assembling ATM cells**, see col. 6, lines 9-27 and element 130, Fig. 5) in connection with the communication channel (**communication channel for data coming into data paths of the Buffering and Routing unit 126**, see data arrow coming into element 126, Fig. 7);

a status location budget manager (**Buffer Manager unit**, see element 128, Fig. 7) in connection with the cell assembly unit (**Buffer Manager 128, Fig. 7 in connection with Output Translation, element 130, Fig. 5**);

at least one cell accumulation buffer (**one of data paths #1, #2, #3, #4, Fig. 7**) in connection with the status location budget manager (**in connection with Buffer Manager unit, see element 128, Fig. 7**);

a slot assembly unit (**Cell Buffer Memory 174, Fig. 7**) in connection with the at least one cell accumulation buffer (**in connection with data paths #1, #2, #3, #4, col. 7, lines 38-48, Fig. 7**) and said second memory controller (**Memory Manager #2, element 172 Fig. 7**); and

at least one address pool (**Free List Memory**, element 176, Fig. 7) in connection with the status location budget manager (**in connection with Buffer Manager unit, element 128, Fig. 7**), the slot assembly unit (**Cell Buffer Memory 174, Fig. 7**), and the data output section (**outgoing data from data paths, Fig. 7**);

wherein the slot assembly unit (**Cell Buffer Memory 174**, Fig. 7) receives cells (**receives ATM cells**, col. 7, lines 49-67, col. 8, lines 1-10 and Fig. 7) from the at least one cell accumulation buffer (**from data paths**, col. 7, lines 38-48, Fig. 7) and package the received cells into cell slots (**the cells received are stored in cell slots**, Fig. 10) to be stored in the second memory (**ATM cells for ports 7-15 are stored in the respective memory buffers located in the Cell Buffer Memory element 126 pointed to by Pointer Memory 180**, see col. 7, lines 25-37 and Figs. 7 and 10).

*Response to Arguments*

5. Applicant's Remarks/Arguments filed on 1/24/2006 have been fully considered but they are not persuasive.

Applicant argued on page 3, second and third paragraphs of applicant's Remarks that Headrick fails to disclose or suggest that "the data input section further comprises at least one cell accumulation buffer and a slot assembly unit, the slot assembly unit being configured to receive cells from the at least one cell accumulation buffer and package the received cells into cell slots to be stored in the second memory," the Examiner respectfully disagrees.

Applicant's attention is directed to the data input section as shown in Headrick's Fig. 7 that comprises data paths #1, #2, #3, #4 (the data input section that comprises at least one cell accumulation buffer, Fig. 7) and a Cell Buffer Memory 174 (a slot assembly unit, Fig. 7) being configured to receive ATM cells (receives cells, col. 7, lines 49-67, col. 8, lines 1-10 and Fig. 7) from data paths (from the at least one cell accumulation buffer, col. 7, lines 38-48) and package the received cells into cell slots (the cells received are packaged by the Cell Buffer Memory to be

stored in cell slots, Fig. 10) to be stored in the second memory (ATM cells for ports 7-15 are packages to be stored in the respective memory buffers located in the Cell Buffer Memory element 126 pointed to by Pointer Memory 180, see col. 7, lines 25-37 and Figs. 7 and 10). This reads on the newly added limitations recited in claim 1 and thus Headrick teaches all of the elements applicant argued Headrick fails to disclose or suggest.

In light of the foregoing, claims 1-10 stand rejected under 35 U.S.C. 102(e) as being anticipated by Headrick et al. (USP 5,724,358). Claim 11 is rejected in view of a new ground of rejection under 35 U.S.C. 102(e) as being anticipated by Headrick as well.

*Allowable Subject Matter*

6. Claims 12-16, 18-26, 28, 31-33 are allowed.

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if the 35 U.S.C. 112, second paragraph rejection set forth to claim 29 above can be overcome.

The following is a statement of reasons for the indication of allowable subject matter:

In claim 12, a network switch as recited in claim 6, wherein the data output section further comprises:

- a cell disassembly unit in communication with the communication channel;
- a cell retrieval and reclaim unit in communication with the cell disassembly unit; and
- a read buffer and slot disassembly unit in communication with the cell retrieval and reclaim unit and the second memory controller.

In claim 17, a network switch as recited in claim 7, wherein said at least one address pool further comprises

- a cell free address pool connected to the first memory controller; and
- a slot free address pool connected to the second memory controller.

In claim 28, a method for storing data in a network switch, said method comprising the steps of:

- determining if a cell count is less than a first predetermined threshold for the egress;
- determining if a number of cells in the second memory is zero; and
- determining if a number of cells in the first memory added to a number of cells remaining in an assembly is less than the first predetermined threshold.

In claim 29, a method for storing data in a network switch, said method comprising the steps of:

initializing a cell count;  
setting an in progress flag;  
loading a first cell pointer into a memory controller;  
incrementing the cell count;

In claim 30, a method for storing data in a network switch as recited in claim 29, further comprising the steps of:

determining if a last cell bit is set; and  
loading a next cell pointer and continuing to store cells if the last cell bit is determined not to be set.

In claim 31, a method for storing data in a network switch, said method comprising the steps of:

wherein the step of storing data in the second memory further comprises the steps of initializing global storage of data and continuing global storage of data until a last slot is stored.

### ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Duong can be reached on 571-272-3164. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**FRANK DUONG  
PRIMARY EXAMINER**

Kevin Mew  
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